Electronic Version
Stylesheet Version v1.1.1

Claims

[c1] What is claimed is:

1.An electrically programmable non-volatile memory cell, comprising:

a semiconductor substrate of first conductivity type;

a pair of spaced apart source/drain (S/D) regions defined on said semiconductor substrate;

a channel region between said source/drain (S/D) regions;

a first dielectric layer disposed on said source/drain (S/D) regions;

an assistant gate stacked on said first dielectric layer, wherein said assistant gate has a top surface and sidewalls;

a second dielectric layer comprising a charge-trapping layer uniformly disposed on said top surface and sidewalls of said assistant gate and disposed on said channel region, wherein said second dielectric layer produces a recessed trough between said source/drain (S/D) regions; and

a conductive gate material filling said recessed trough for controlling said channel region;

wherein, in operation, said assistant gate is biased to a

voltage V_i that is sufficient to induce a corresponding inversion region of second conductivity type in said semiconductor substrate; and wherein said inversion region of second conductivity type functions as a source/drain of said electrically programmable non-volatile memory cell.

[c2] 2.The electrically programmable non-volatile memory cell according to claim 1 wherein said first dielectric layer is made of silicon dioxide.

[c3] 3.The electrically programmable non-volatile memory cell according to claim 2 wherein said silicon dioxide is thermally grown.

[c4] 4.The electrically programmable non-volatile memory cell according to claim 1 wherein said second dielectric layer is a tri-layer dielectric.

[c5] 5.The electrically programmable non-volatile memory cell according to claim 1 wherein said second dielectric layer is an ONO tri-layer, and said charge-trapping layer is a silicon nitride layer sandwiched between a bottom oxide layer and a top oxide layer.

[c6] 6.The electrically programmable non-volatile memory cell according to claim 1 wherein said second dielectric layer is a bi-layer dielectric.

[c7] 7.The electrically programmable non-volatile memory cell according to claim 1 wherein said assistant gate is made of polysilicon.

[c8] 8.The electrically programmable non-volatile memory cell according to claim 1 wherein said conductive gate material comprises polysilicon.

[c9] 9.The electrically programmable non-volatile memory cell according to claim 1 wherein said conductive gate material is metal.

[c10] 10.The electrically programmable non-volatile memory cell according to claim 1 wherein said inversion region of second conductivity type is electrically connected to a pickup well that is formed in said semiconductor substrate at one end of said assistant gate and partially overlaps with said assistant gate, and wherein said pickup well is biased to a bit line voltage.

[c11] 11.An electrically programmable non-volatile memory cell, comprising:
a semiconductor substrate;
a pair of spaced apart source/drain (S/D) regions defined on said semiconductor substrate;
a channel region between said source/drain (S/D) regions;

a first dielectric layer disposed on said source/drain (S/D) regions;

an assistant gate stacked on said first dielectric layer, wherein said assistant gate has a top surface and side-walls;

a second dielectric layer comprising a charge-trapping layer uniformly disposed on said top surface and side-walls of said assistant gate and disposed on said channel region, wherein said second dielectric layer provides a recessed trough between said source/drain (S/D) regions; and

a conductive gate material filling said recessed trough.

[c12] 12.The electrically programmable non-volatile memory cell according to claim 11 wherein, in operation, said assistant gate is biased to a voltage V_i that is sufficient to induce a corresponding inversion region in said semiconductor substrate; and wherein said inversion region functions as a source/drain of said electrically programmable non-volatile memory cell.

[c13] 13.The electrically programmable non-volatile memory cell according to claim 11 wherein said first dielectric layer is made of silicon dioxide.

[c14] 14.The electrically programmable non-volatile memory cell according to claim 11 wherein said second dielectric

layer is an ONO tri-layer, and said charge-trapping layer is a silicon nitride layer sandwiched between a bottom oxide layer and a top oxide layer.

[c15] 15.The electrically programmable non-volatile memory cell according to claim 11 wherein said assistant gate is made of polysilicon.

[c16] 16.The electrically programmable non-volatile memory cell according to claim 11 wherein said conductive gate material comprises polysilicon.

[c17] 17.The electrically programmable non-volatile memory cell according to claim 11 wherein said conductive gate material comprises metal.